0 The Intermediate Silicon Tracker

0.1 Introduction

To reach the full physics capabilities of the HFT, PIXEL requires tracks with good pointing resolution at its outer layer and an as good as possible track finding efficiency. TPC tracks alone provide a pointing resolution of around 1000 um at the outer layer of PIXEL which then leads to a single track finding efficiency of about 50%. The SSD layer at a radius of 23 cm improves the pointing resolution to around 400um in the bending direction with an efficiency of a little over 80%.

In principle the HFT with the SSD alone would provide sufficient pointing resolution and single track finding efficiency. However, there would be no redundancy against failing of (parts) of the SSD. Since the SSD is an aging detector this is considered to be an unacceptable risk to the physics program of the HFT. A relatively simple tracking layer between the SSD and the outer layer of the PIXEL should be able to correct this deficiency.

The Intermediate Silicon Tracker (IST) will provide space points with high accuracy in the bending direction while not degrading the single track finding efficiency by more than a few percent because of the added material. The IST will make use of silicon pad sensors with strip-like pads located at a radius of 14 cm. Various technical details draw to a large extent from previous experience on the design and operation of silicon tracker systems such as the PHOBOS silicon tracker stations. The construction of the IST will make use of existing equipment and infrastructure from the PHOBOS silicon tracker through the MIT group.

0.2 Requirements

0.2.1 Overview

The IST must meet a number of tracking requirements and should also be able to cope with the experimental constraints.

The best figure of merit for the tracking capabilities is the final D0 reconstruction efficiency. However, determining this efficiency involves very time consuming and labor intensive GEANT simulations and analysis. The choices that are presented here to meet the requirements are based on a much more simplified tracking code which has successfully been checked against the full calculations in a number of major cases. This simplified code was used to determine the optimum radius of the IST barrel and the internal geometry of the silicon pad sensors.

The most important of the experimental constraints are data rate taking capabilities, radiation levels and the material budget. The data rate and radiation levels are largely a given from RHIC and have to be taken into account in the sensor and readout chip choice. The material budget is

intertwined with the tracking capabilities of the inner tracking system, but has also a large impact on the capabilities of more outward located detectors and their associated physics programs. To produce a low mass IST with enough mechanical rigidity has led to the choice of state of the art materials.

0.2.2 Tracking tasks

The Intermediate Silicon Tracker has to be located between the outer layer of the PIXEL detector and the SSD. Taking mechanical constraints into account this gives a possible radius range from 12 to 20 cm. This radius has to be optimized for reconstruction efficiency while keeping SSD and IST redundancy in mind.

The IST barrel should cover the full acceptance of the STAR TPC, i.e. 2pi coverage for -1<eta<+1. In addition the IST should also be able to accommodate some of the z-range of the interaction point.

At the highest RHIC energy of 200 GEV for Au+Au the charged particle density at a radius of 12 cm can easily exceed 1 per cm^2. The internal structure of the silicon sensors has to be chosen such that the occupancy does not exceed the few percent level.

0.2.3 Tracking efficiency

The tracking efficiency is defined as the percentage of correct single tracks found by the inner tracking system when presented with events with only one track. This efficiency can be found by a full simulation with GEANT and the STAR tracking analysis. A faster way is to calculate the efficiency with the more simple code described in section XXX. This code calculates the efficiencies for 750 MeV/c kaons which is important because these are the particles that need to be tracked for D0 reconstruction. The whole inner tracking system should have an single track efficiency of better than 80%. If the SSD or the IST is not able to provide a proper space point for the track, because of less than 100% coverage or broken channels, then the efficiency should still be above 70%.

0.2.4 Data taking rate

The IST should be able to operate without significant event pile-up for 200 GeV Au+Au collisions. Therefor the IST has to be able to resolve interactions from each beam bunch crossing which are occurring every 116 ns. The spin program at RHIC relies on individual beam bunch crossings to set and determine the relative spin orientations in the proton beams. Also here the IST should be able to resolve individual beam bunches. This has to be quantified better.....

0.2.5 Radiation environment

Extrapolating the radiation doses received by the RHIC experiments during the past RHIC operations, it is expected that the total radiation dose for the IST barrel will not exceed 30 kRad per year [REF needed]. Both the silicon sensors and the readout chips on the hybrids are required to be fully operational after 10 years of operation.

0.2.6 Low mass and mechanical stability

The mass requirements for the IST are defined by the heavy ion physics requirements in the mid-rapidity region and by the W−boson spin physics program for more forward rapidities. The heavy ion vector meson program, going to di-electrons, was marginal given the mass of the SVT when it was still installed in the mid-rapidity region. Similarly, the upsilon program was marginal with the SVT. The PIXEL plus IST should thus strive to be much thinner than the current azimuthally averaged 4.5% radiation lengths of the SVT. The W−physics spin program was hindered by SVT support structures in the pseudo-rapidity region of 1 < < 2. Support structures for the inner tracking system should be designed to reduce mass in this region. To make the Multiple Coulomb Scattering comparable to the detector resolution the thickness of the IST layer should be less or equal 1.5% of a radiation length. This needs quantification

0.3 Design choices

0.3.1 Barrel radius and layout

The efficiency of the whole inner tracking system is determined by an intricate interplay of the detector layer radii, resolutions and thicknesses. Since these characteristics are mostly fixed for PIXEL and SSD, varying the radius of the IST barrel for a certain internal sensor geometry makes it possible to optimize the radius with respect to the single track efficiency quickly. Figure .... shows a calculation for a promising internal geometry. Although the dependence is rather weak it is clear that 14 cm will give the best efficiency. Not too surprising is that this is roughly halfway between the outer layer of PIXEL and the SSD.

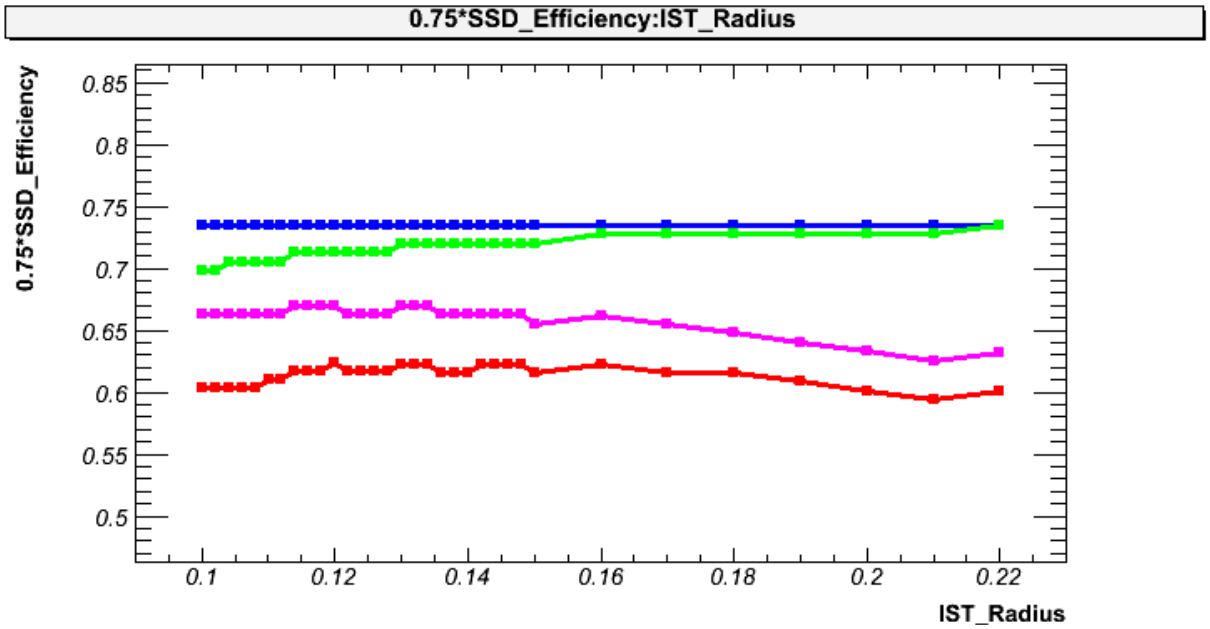

Figure ...: Single track efficiency as function of the IST barrel radius. The assumed internal sensor geometry was 600um in r-phi and 6000um in z. We need a new figure here!

The rest of the layout of the layout of the IST barrel is for the most part determined by the size of the sensors and the requirement of 2pi coverage for -1<eta<+1. Figures ... and ... show an X-Y cross section of the inner tracking system and a 3d rendering of the IST barrel, respectively. For the anticipated sensor layout there will be 24 layers tiled to give 2pi coverage. The barrel will be 62 cm long and cover -1.5<eta+1.5.

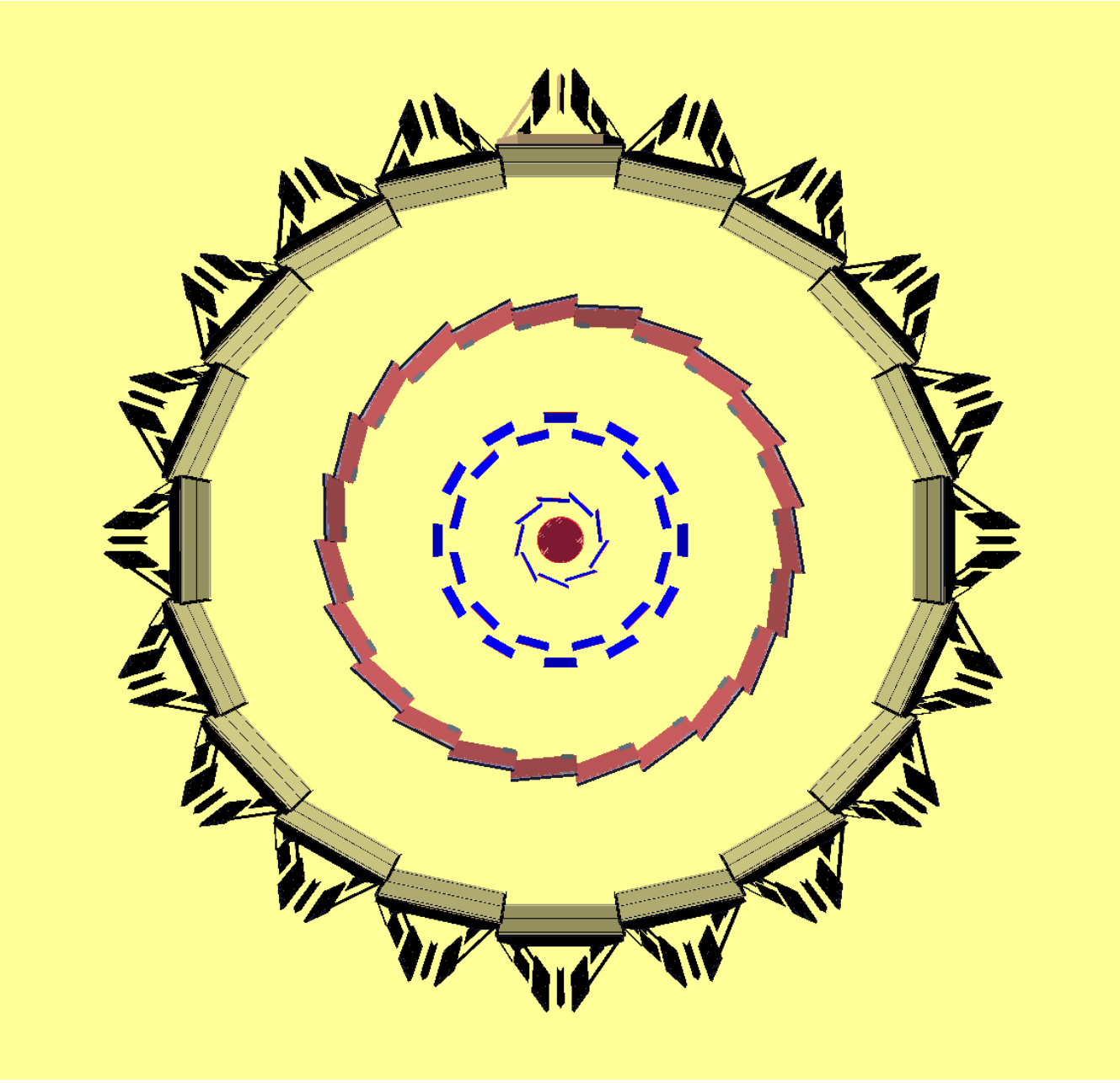

Figure ...: View along the beam axis showing from inside to outside; the beampipe, 2 PIXEL

layers, 1 IST layer and 1 SSD layer. New picture needed, PIXEL is OLD

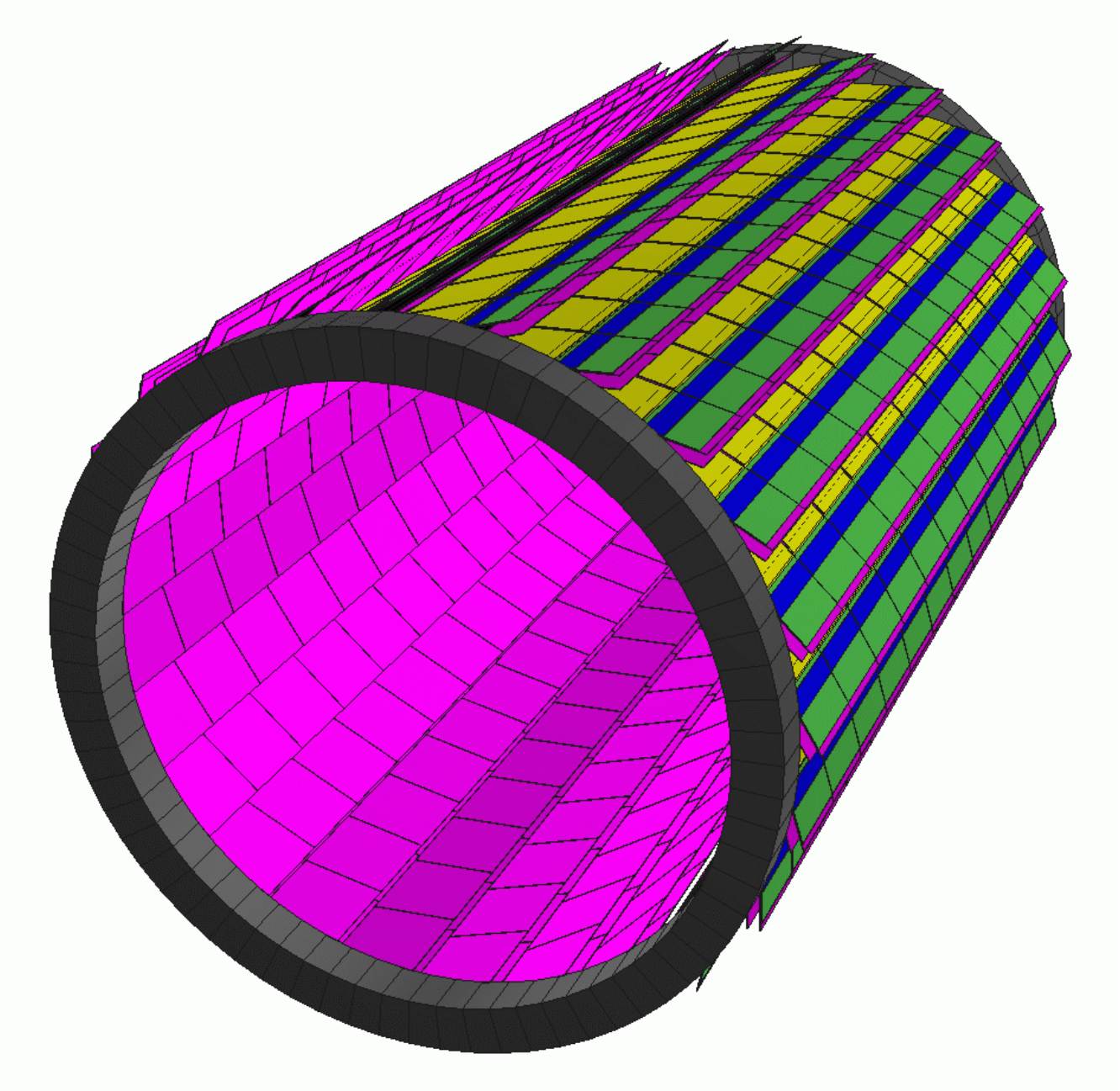

Figure ...: IST barrel layout with 24 ladders of 62 cm long at a radius of 14 cm.

0.3.2 Silicon detectors

The manufacturing techniques for silicon sensors are well established and are mastered by several manufacturers. The preference is to produce single sided devices with p-implants on n-bulk silicon and poly-silicon biased. They are relatively easy to produce with high yields and can also be handled without much difficulty in a standard semi-conductor lab. In contrast, double-sided devices have lower yields (thus more expensive) and need special equipment to

handle them.

Central Au+Au collisions at 200 GeV lead to a particle density of about 1 per cm^2 at the IST barrel near mid-rapidity. Using silicon strip sensors would lead to unacceptable occupancies and double hit probabilities.

Silicon pad sensors are much better suited to this environment and proved their suitability in the PHOBOS experiment. Figure ... shows a study of the single track finding efficiency of the whole HFT as a function of the pad layout of the IST sensors. The better resolution (the size of the pads on the y-axis) is in r-phi, the bending plane. From these studies it was determined that 512 channels arranged in strips of roughly 600um X 6000um give an acceptable efficiency of about 83%. Going to more channels could give a slightly better efficiency but would lead to space problems when trying to mount more readout chips on the hybrids. The left plot shows the efficiency when hits from the SSD are not included in the tracking. This could happen because of small gaps in the SSD acceptance or broken channels. This study shows that the single track finding efficiency goes to 73%. This has to be compared to 50% if the IST would not be there and only the TPC would provide tracking to the PIXEL. The IST greatly adds to the redundancy of the inner tracking system.

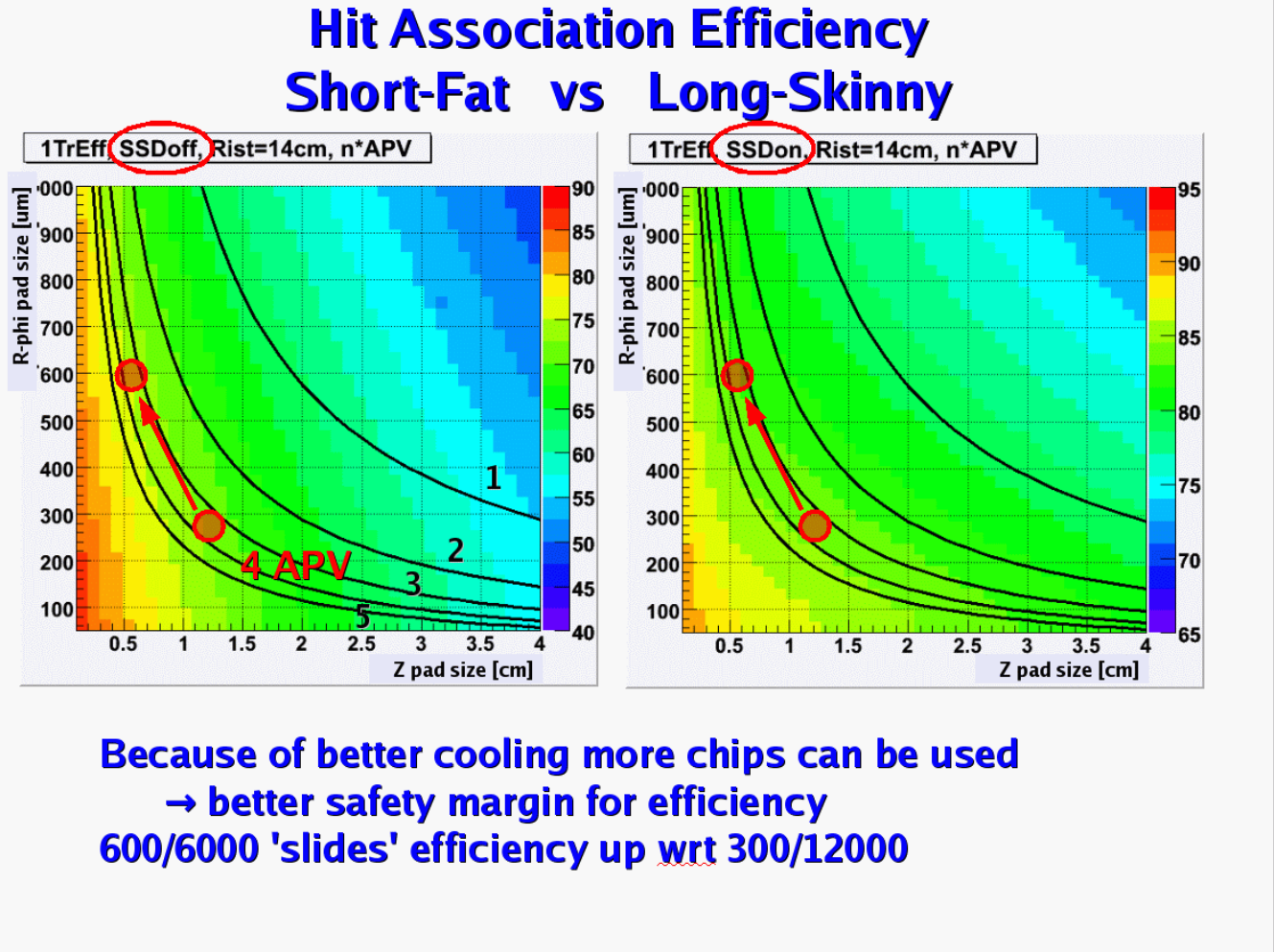

Figure ...: Single track finding efficiency for different r-phi and z pad sizes of the IST. The solid lines show the iso-lines for certain amount of channels (1 = 128ch, 2 = 256ch, 3 = 384ch, 4 =

512ch, 5 = 640ch). The left picture shows the efficiency when no hits from the SSD are included , in the right picture the SSD hits are included in the track. Particles tracked are kaons at 750MeV/c. (NEED NEW PICTURE)

Figure ... shows the internal layout of the IST silicon pad sensors. The active elements are arranged in such a way that the best resolution is in the bending direction, I.e. r-phi. Along the beam direction the resolution will be ten times larger. The sensors will be roughly 10 cm X 4 cm with 1024 channels. All channels are AC coupled and connected through a second metal layer to bonding pads on one long edge of the sensor. From the manufacturing point of view this design is reasonably standard. Preliminary discussions with Hamamatsu showed that they are able to produce the proposed sensors within the proposed budget.

Hamamatsu is the preferred vendor because of their excellent track record with respect to the quality of their produced sensors. This will greatly reduce the amount of quality control that has to be performed for these sensors. It will be sufficient to fully measure the characteristics of one or two samples per produced batch of about 20 sensors. Moreover, Hamamatsu uses design rules which make their sensors relatively radiation hard. Therefor we foresee no serious performance degradation during the sensor lifetime.

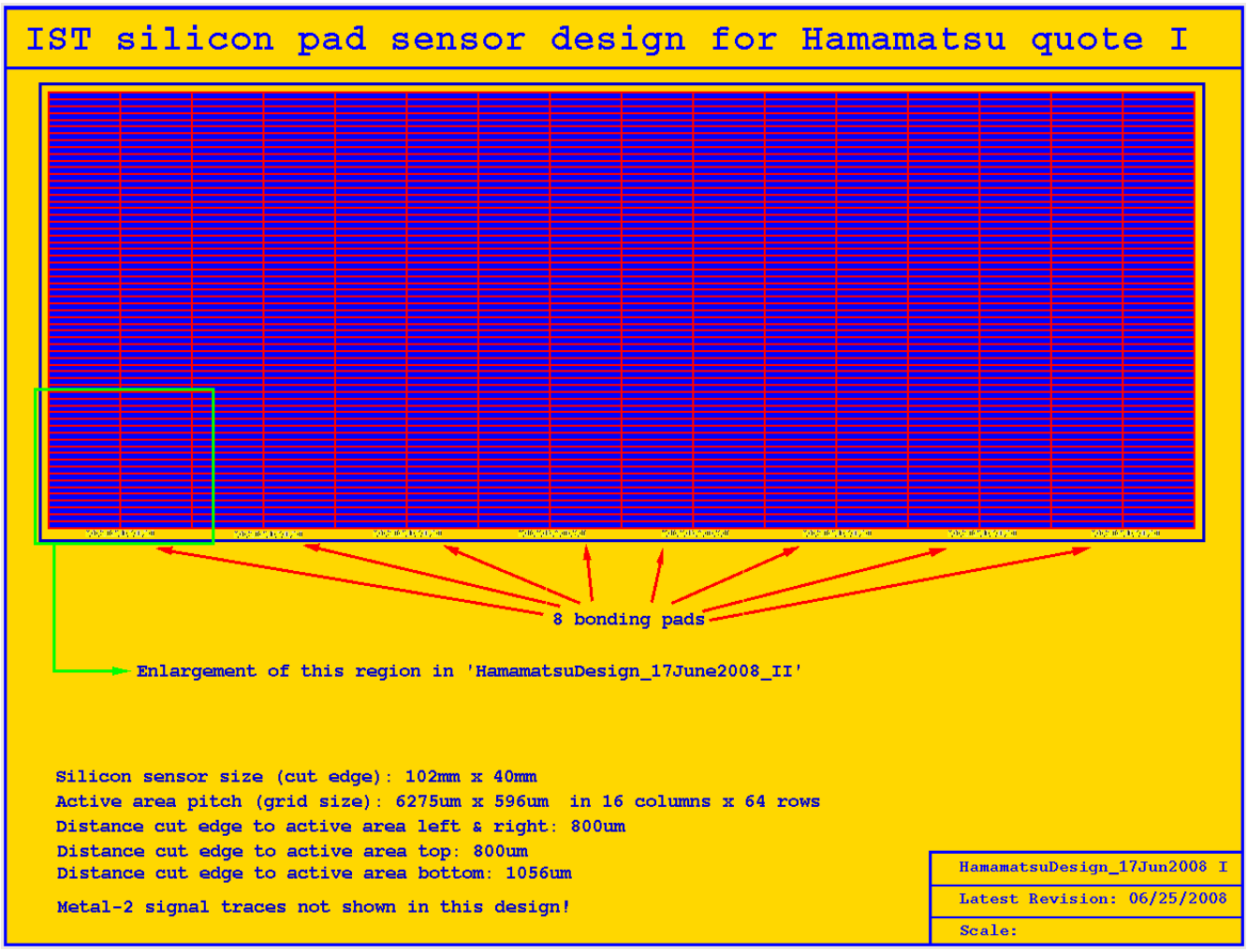

Figure ...: IST silicon pad sensor internal layout.

0.3.3 Read-out chips

About 150,000 channels will be read out in the IST. Readout chips with the necessary requirements for this system are already being used for similar purposes by other experiments. We chose the APV25-S1 readout chip which was designed for the CMS silicon tracker and of which about 75,000 will be used in CMS [REF User Manual and NIM paper]. Each channel of the APV25-S1 chip consists of a charge sensitive amplifier whose output signal is sampled at 40 MHz which accounts for the LHC interaction rate. The samples are stored in a 4 μs deep analog pipeline. Following the trigger the data in the pipeline can be processed by an analog circuit, mainly de-convoluting the amplifier response from the actual signal and associating the signal with a certain interaction (or rather beam crossing at LHC). The resulting analog data can then be multiplexed and sent to digitizer boards. Although the analog data leads to higher data volumes at the front-end, it is an enormous advantage that charge sharing between strips and common mode noise can be studied in detail, which greatly improves the understanding and performance of the detector. The Equivalent Noise Charge (ENC) of the APV25-S1 depends on the capacitance of the strips and the de-convolution algorithm used, but, for our purposes, it is better than 2000 electrons. With 300 μm thick silicon sensors this will give a signal-to-noise ratio of better than 11:1 when we take the most probable energy deposition by a minimum ionizing particle (MIP). The nominal power consumption of the APV25-S1 is 2.31 mW/channel, i.e. about 0.3 Watt/chip. The chips are fabricated in the radiation hard deep sub-micron (0.25 μm) process. Figure ... shows a close-up view of the APV25-S1 chip.

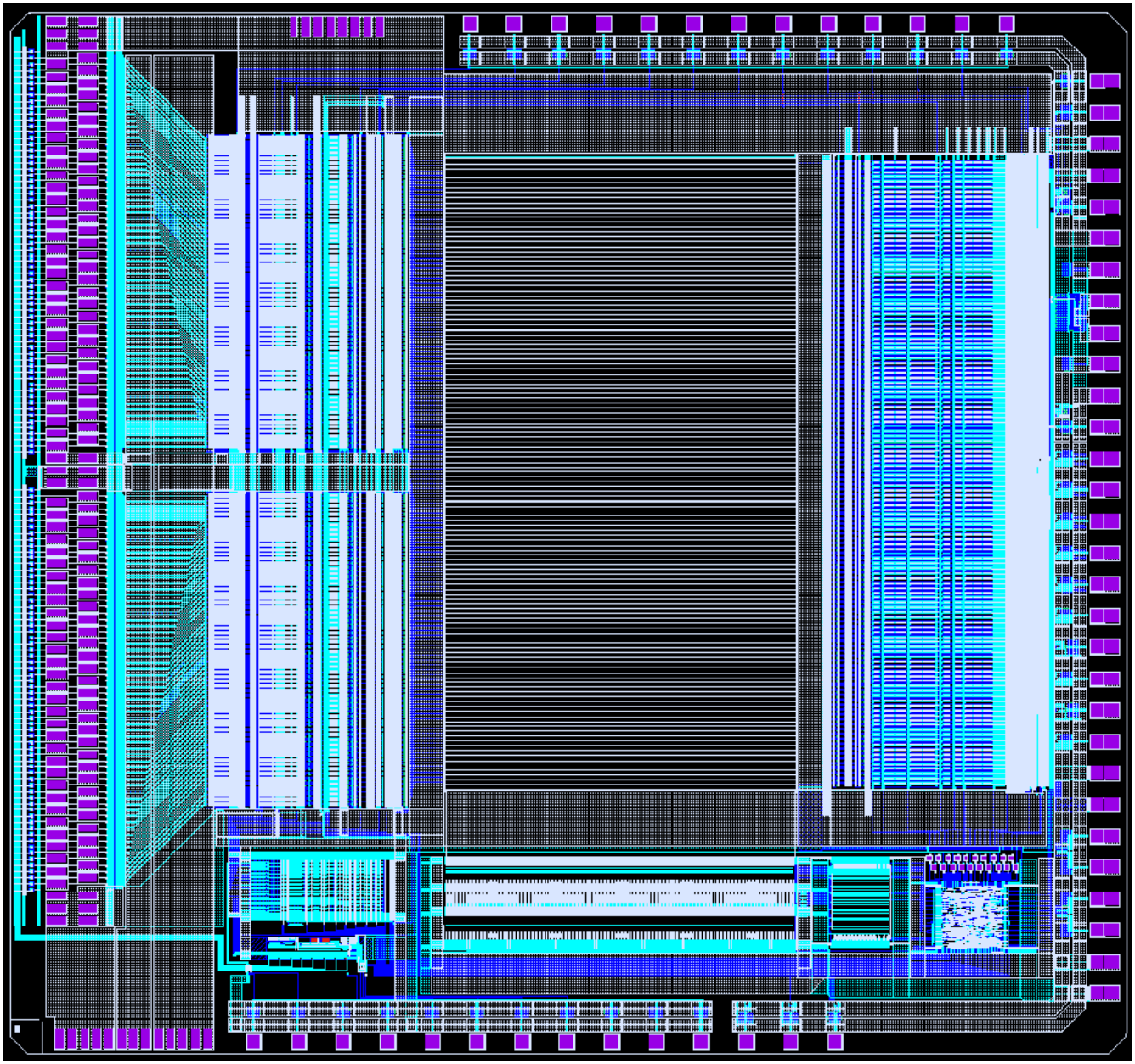

Figure ...: Close-up of the APV25-S1 chip of which the IST will use about 1200.

0.3.4 Hybrids and modules

To keep the material budget low the IST hybrids and modules have to constructed from low mass materials. Figure ... shows a promising prototype Kapton hybrid design with integrated long Kapton cable. Both hybrid and cable are about 100um thick. The hybrid will have to be laminated onto a proper substrate material to achieve enough mechanical rigidity. Carbon-Carbon and carbon fiber are being prototyped to study their mechanical and thermal properties. In the final design the flexible cable will be long enough to reach the readout electronics outside the TPC area (~400cm) or to reach a connection to more standard cables outside the active areas which are sensitive to too much material (~100cm). Both lengths pose no production problems. The main concern is the electrical characteristics of the long cable, this is under

investigation. The hybrid in Figure ... has been taken into production.

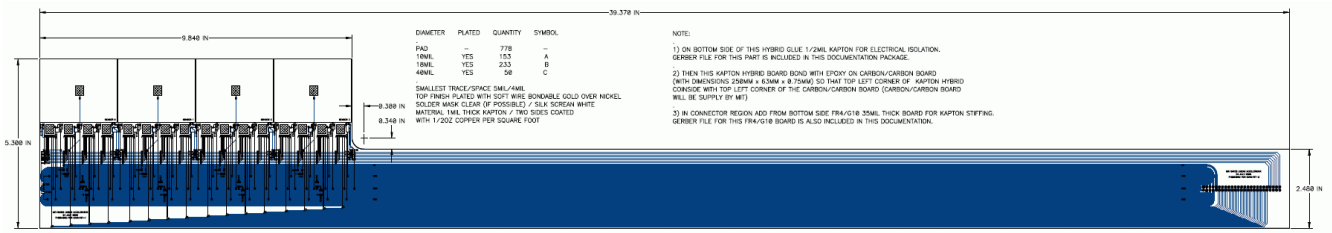

Figure ...: IST hybrid (left) and cable (right) assembly.

The layout of an IST module can be seen in Figure ...**.** The hybrid carries 2 sensors of the type shown in Figure ... and 16 readout chips. There will be a gap of 400um between the sensors. Overlapping the sensors would lead to too many assembly complications. These acceptance gaps will be compensated because of the redundancy between SSD and IST. An interesting feature, and which is not visible in this picture, is that the cable will be folded over to the backside of the ladder on which this module will be mounted. In this way the cables are neatly tucked away and do not obscure visual access to the modules, which is needed for spatial survey purposes and inspection.

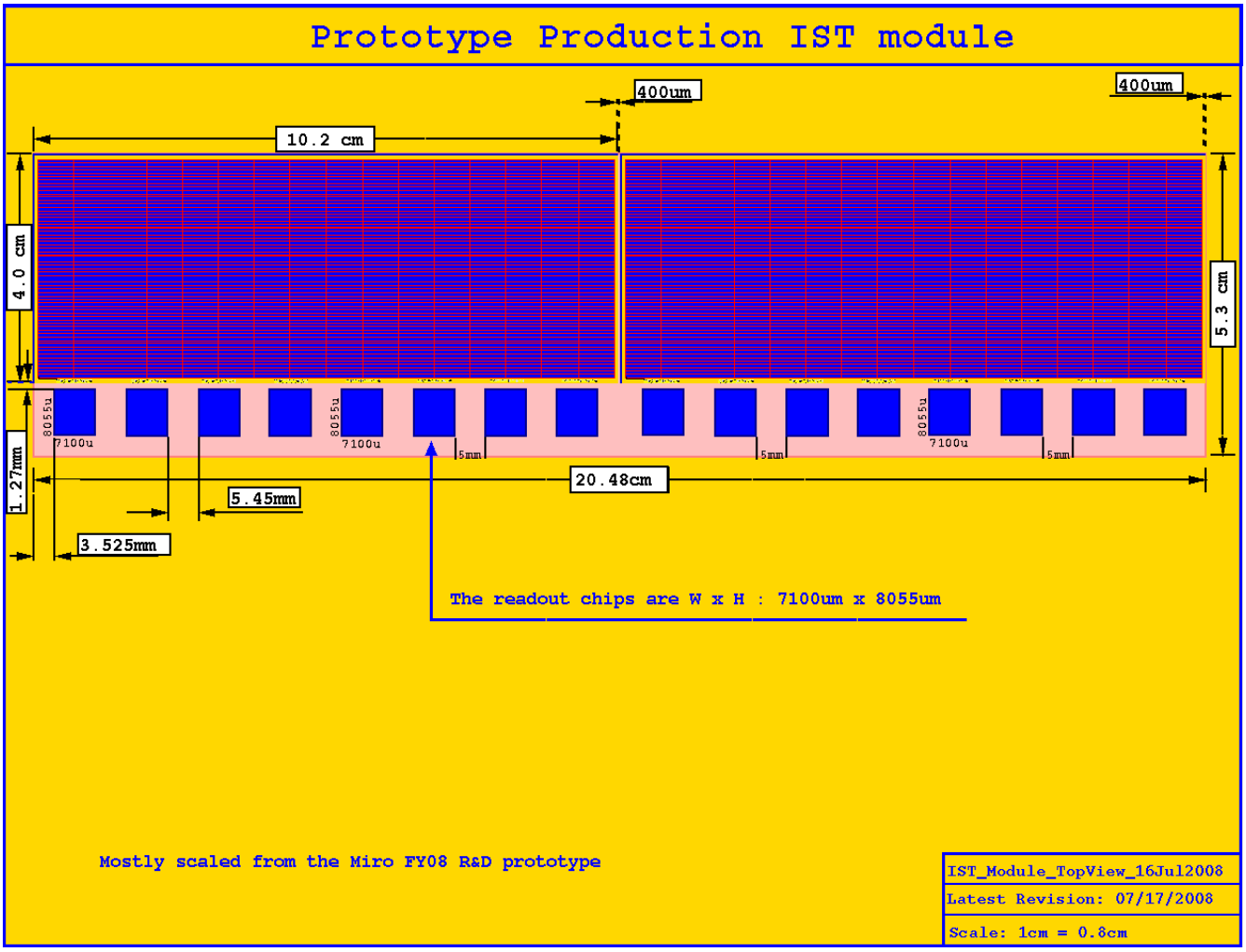

Figure ...: Layout of an IST module. Note that this is a prototype, other picture?

0.3.5 Mechanical support structure

The IST barrel will consist of 24 ladders which get mounted on a carbon fiber support cylinder. The Inner Support Cylinder (ISC) is described elswhere in this document (REF) and has not been taking into account in the material budget calculations.

Figure ... shows the ladder structure of the IST with and without the modules mounted. This ladder is a shorter version of the staves which are under development for the ATLAS tracking upgrade (REF). Because they are shorter they are even more rigid than the ATLAS staves and it is expected that their midpoint sag will be less than 100um when only end supports are used. A prototype ladder is being produced and will be tested.

A more detailed cross section of the ladder and mounted modules can be found in Figure .... This design shows the 300um thick silicon sensor, the 300um thick APV25-S1 readout chip, the 100um thick kapton hybrid-cable, the 500um thick Carbon-Carbon substrate and the 5mm thich carbon fiber ladder with cooling tube. It also shows nicely how the kapton folds over to the backside of the ladder where it is routed out to the readout system. The Carbon-Carbon

substrate not only gives mechanical rigidity to the module, but also acts as a heat sink to transport heat from the readout chips to the cooling tube in the ladder.

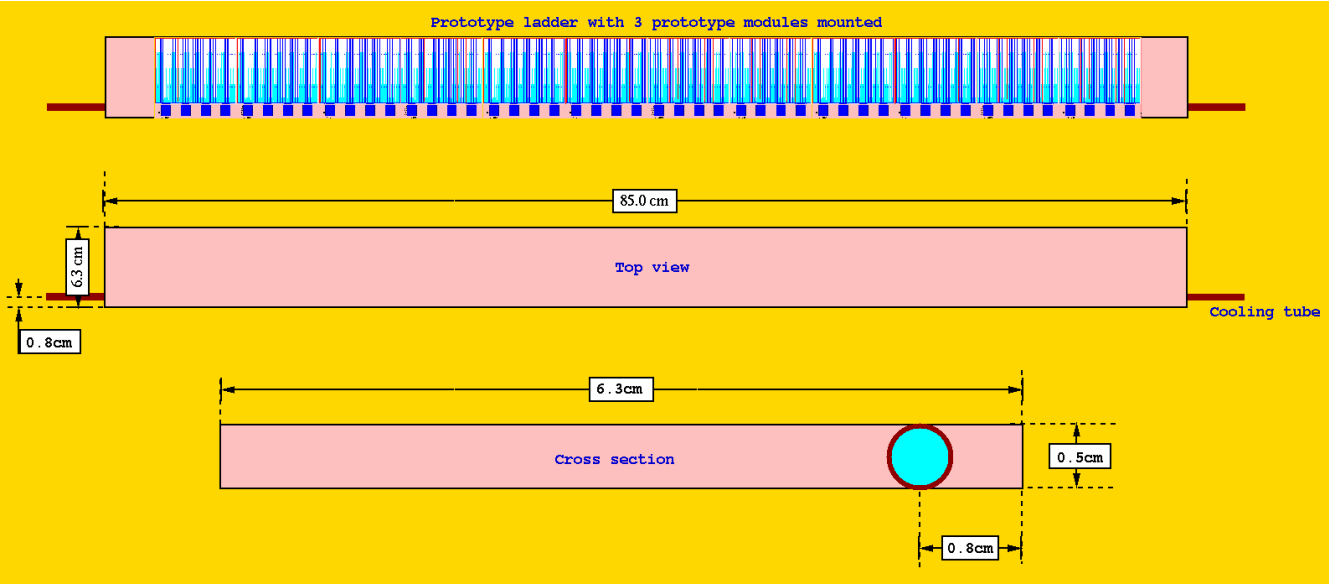

Figure ...: Drawings of the IST ladder. Top picture is with modules attached, middle picture shows the bare ladder and bottom picture shows a cross section of the ladder.

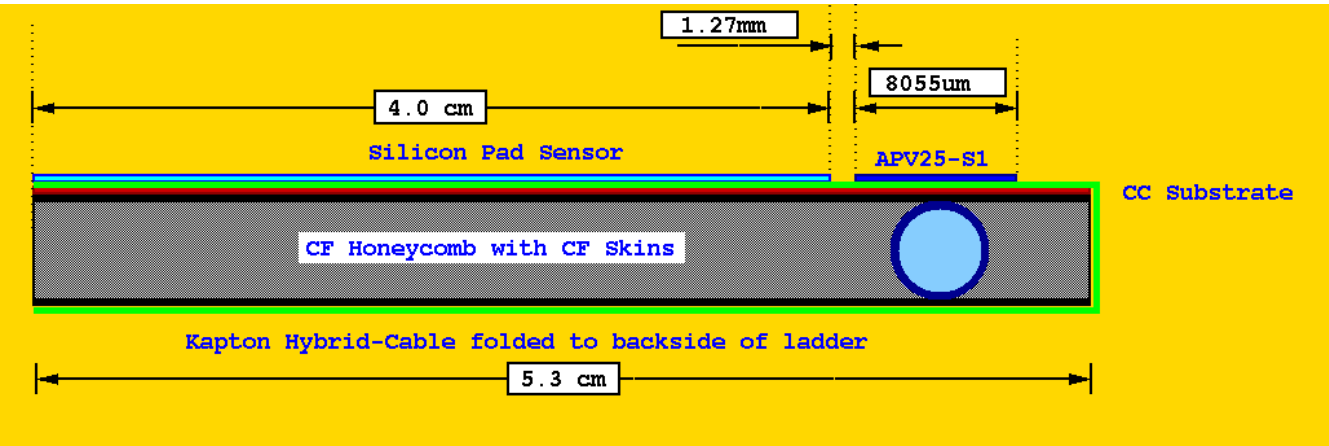

Figure ...: Cross section of the ladder and modules. Especially note the kapton hybrid which gets folded over to the other side.

The options for mounting the ladders on the Inner Support Cylinder are still under investigation. Again it would be benficial to profit from the extensive research that the ATLAS upgrade group has done for the upgrade staves and support. Figure ... gives an artists impression of one of the more promising designs. Here the ladders would be mounted with clips on the ISC. Because of the shorter length of the IST ladders it is probably sufficient to use endpoint supports only. One end of the ladder would be kept fixed while the other end allows thermal expansion. Most likely there will have to be an clamshell interface on which the ladders are mounted first. This clamshell can then be optically surveyed to determine the sensor positions before it gets mounted on the ISC.

The mechanical support structure will be manufactured with an overall accuracy of 100 um. Locally, the structure supporting the IST requires an accuracy of less than 100 um. For instance, the mounting surfaces of the sensor modules will have to be flat to within 50 um to avoid stress, and possibly breakage, of the sensors.

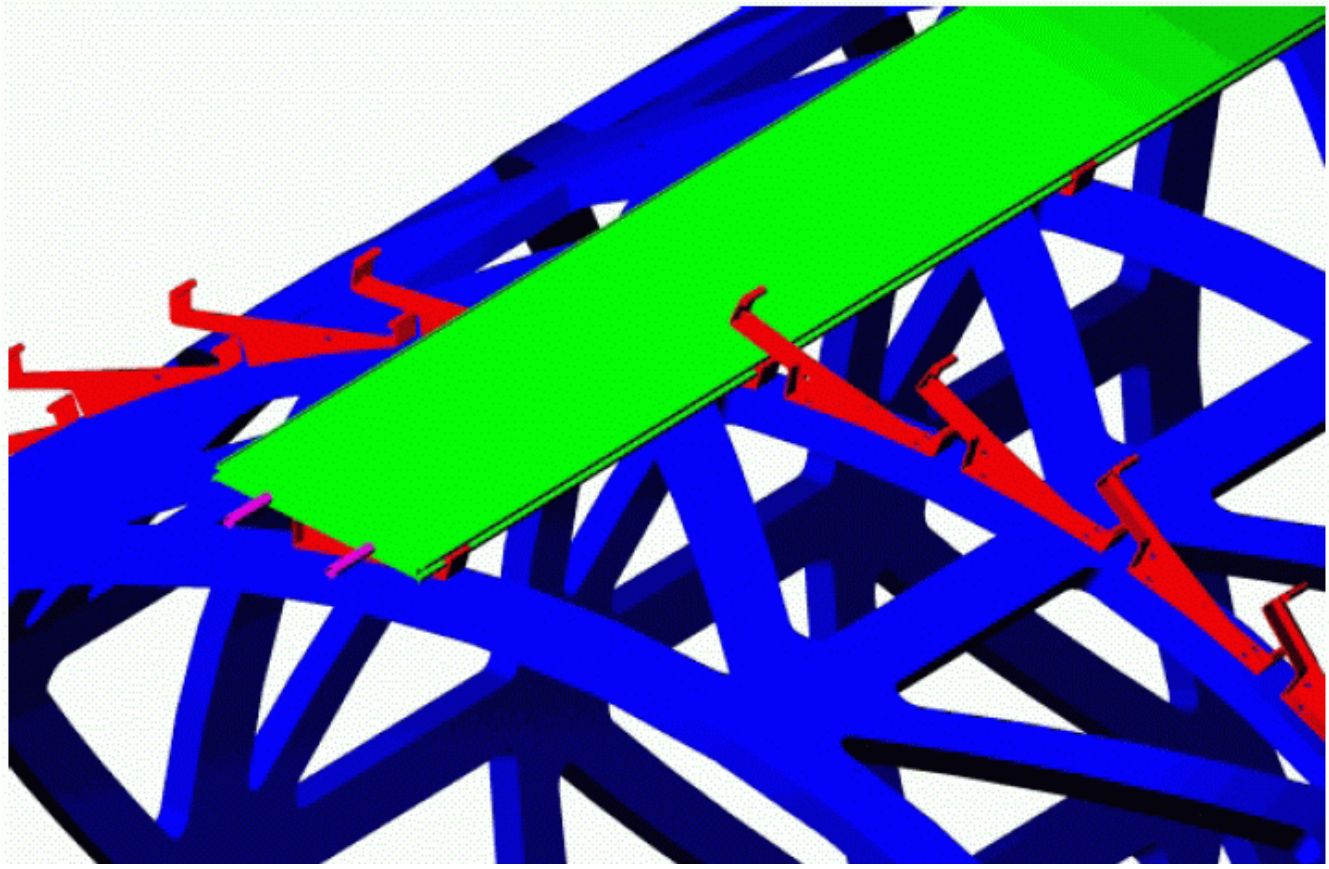

Figure ...: Ladder 'clip' mounting of the IST ladders onto the supporting cylinder (ISC).

Figure ... gives a realistic estimate of the IST material budget by describing ladder and module designs in a GEANT geometry. These results where obtained by propagating 100,000 geantino events through the IST geometry using GEANT 3.21/08. The material budget at mid rapidity is well below the required 1.5% Xo. However, it should be noted that, because of a lack of a design, the ISC and support clips where not included in these calculation. The asymmetry in the material budget is caused by the kapton readout cables only running in negative rapidity direction.

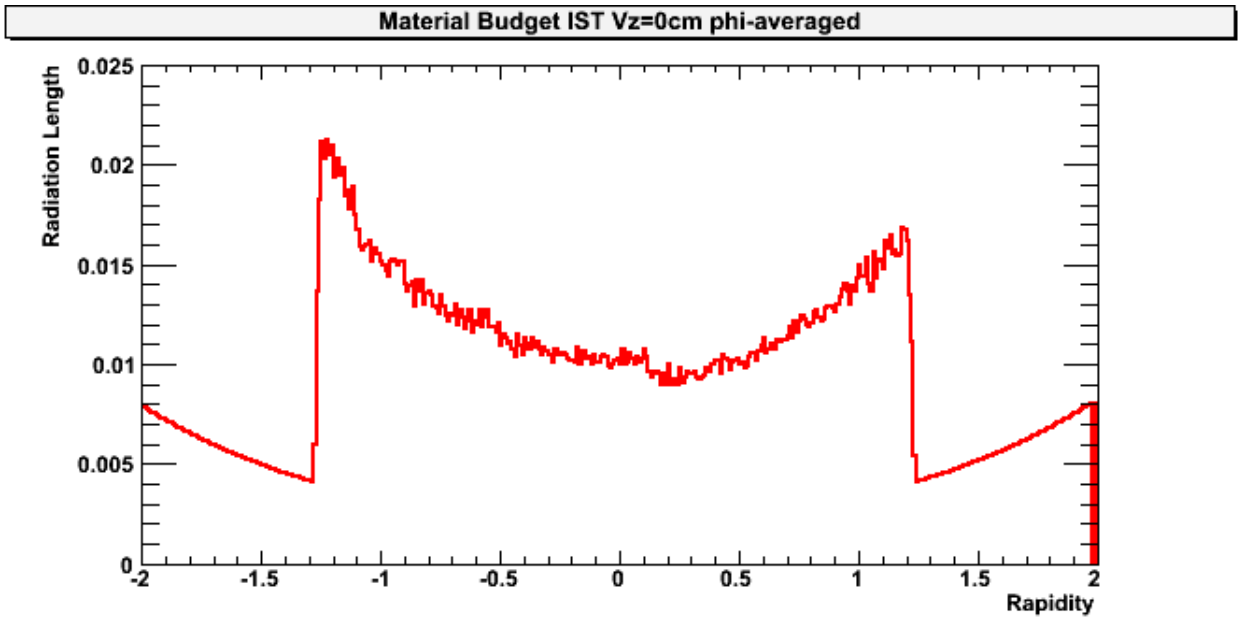

Figure ...: Phi averaged material budget for the IST as a function of rapidity. This needs to be desperately redone!

0.3.6 Cooling

The only source of dissipation on the ladders are the 48 APV25-S1 readout chips. Athough the nominal power consumption is about 300mW per chip, the final power consumption is depending on the capacitance of the attached sensor channels and the optimal settings of the chip parameters. For safety margin reason a maximum dissipation of 400mW per chip is assumed. This leads to a dissipation of about 20 Watt per ladder, 480 Watt for the whole IST barrel. Trying to cool this with air only was considered too daunting and liquid cooling channels were incorporated in the ladder design. The 20 Watt per ladder leads to about 1.2mW per mm^2 dissipation if the heat would spread out isotropically. The placement of the cooling tube directly under the readout chips, see Figure ..., and the use of high thermal conductive material like Carbon-Carbon should make the cooling of the ladders manageable with a room temperature water cooling system.

0.4 Readout system and Slow Controls

0.4.1 Readout system and DAQ interfacing

Three Wiener readout crates, each containing 9 slots, will house the 8x2 read-out boards (RDO) and 1x2 crate controller boards (RCM). These crates, 6U in size and powered by remote supplies, will be mounted on the electronics platform next to the STAR detector. Just outside the inner TPC area there will be transition boxes translating the thin and fragile Kapton cables to more standard detector cables which connect to the RDO. Each RDO handles three detector cables (~ 48 APV chips), providing an ADC, some data buffering and control of APV chip triggering and readout sequencing. The RDO also operates the I2C slow controls interface to the detector. The RCM interfaces to the STAR trigger and DAQ via the ALICE detector data link (DDL) source interface units (SIU), the standard for all new STAR DAQ-connected developments for the DAQ1000, Time of Flight (TOF), Barrel (BTOW), Forward GEM Tracker (FGT) and Endcap (ETOW) tower level 2 upgrade. The readout system, as designed, will be able to transmit data to L2 following the same plans as for TOF, ETOW, FGT and BTOW. A Linux box will be located in the STAR DAQ room and fitted with the ALICE DDL receiver board and a Myrinet interface to the event builder computer. A schematic detailing these connections is shown in Figure ....

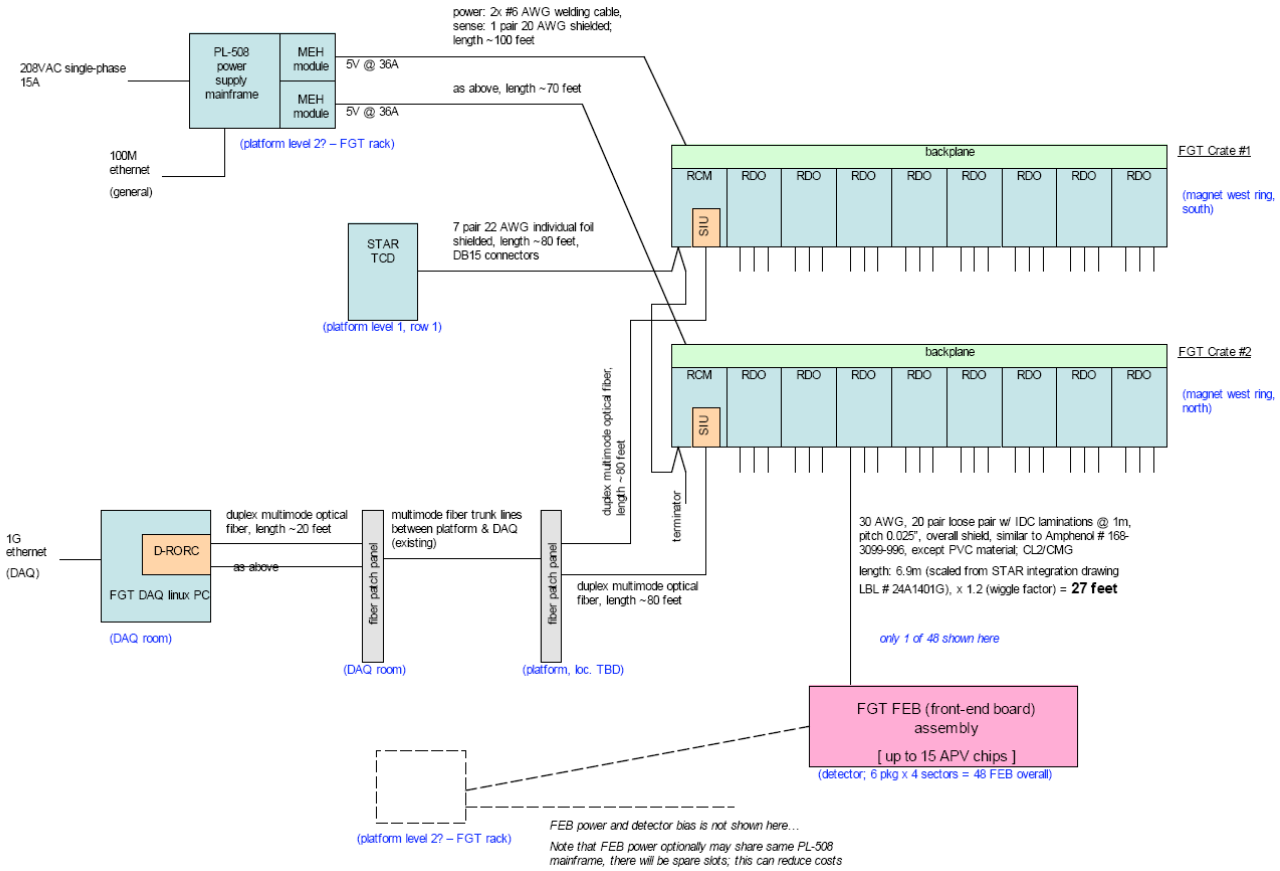

Figure ...: IST DAQ block diagram.

0.4.2 Slow Controls System

The slow controls system will serve as the primary means for controlling and monitoring the working parameters of the IST. These parameters, such as the hybrid temperature, component currents, voltages and gas flow rates, will be interfaced with the standard STAR alarm system. The alarm system logs the parameter history and alerts the shift crew if operating limits are exceeded. The black dashed lines in Fig 53 show the communication flow between the slow controls computer and the hardware being controlled. The red solid lines represent the actual hardware connections which allow this communication. The slow controls for the IST detector and readout crates will be handled exclusively by Ethernet traffic to the IST Linux box, through the ALICE DDL link to the readout crates, and then finally through the RDOs to the APV's via the local I2C link. There will be no other hardware needed for slow controls. All power supplies will be fitted with an Ethernet controls interface.

Although STAR is using EPICS as its standard slow control system there is a slight preference to use LabView instead. Labview provides the user with virtually any instrument driver and a very convenient user interface. LabView runs on bothWindows and Linux. It is relatively simple to interface LabView and EPICS. However, at the moment, both options are still open.

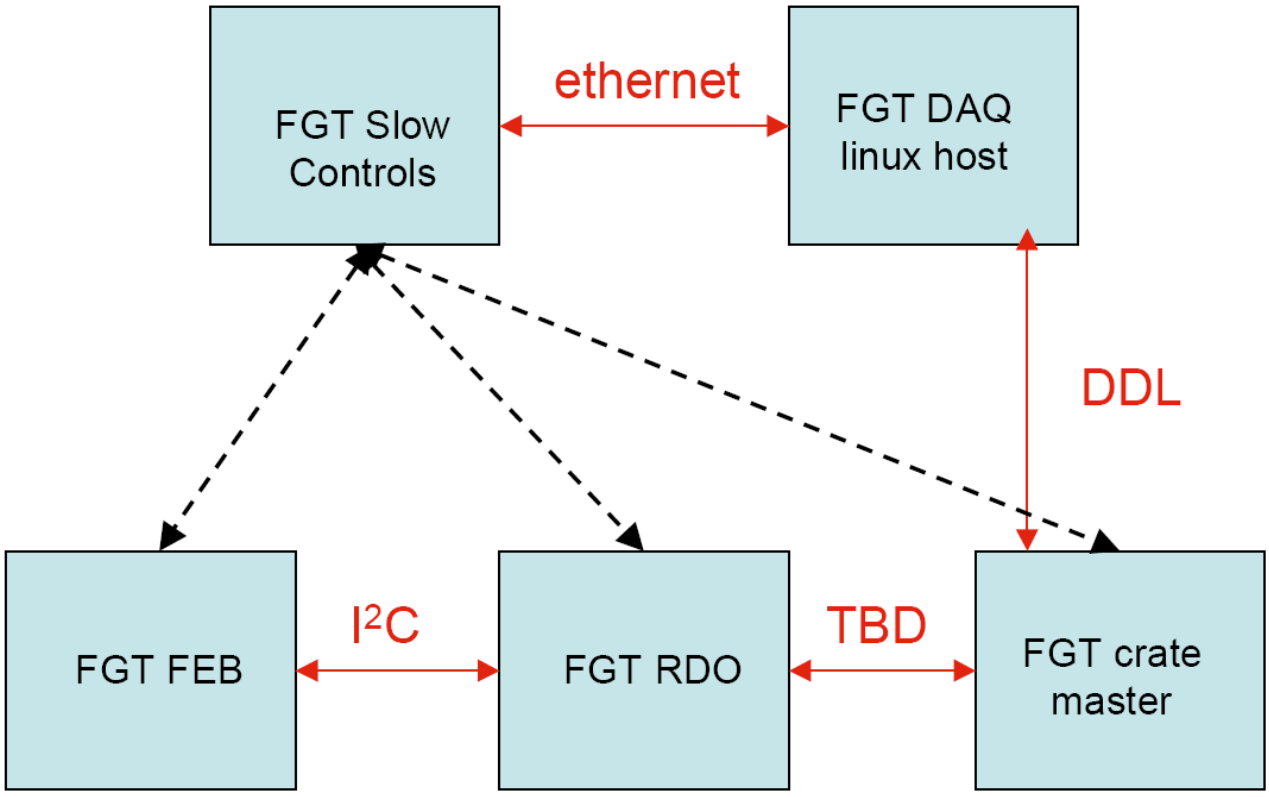

Figure...: IST slow controls flow diagram.

0.5 Spatial survey and alignment

The IST will have to be aligned with respect to the other detector in the inner tracking upgrade, PIXEL and SSD. The final alignment will be done with tracks through an iterative residual method. However, for this method to be successful it is important that the positions of the active elements are known in advance with an accuracy comparable to the resolution of the detectors. For the IST the following 5-step plan has to be followed to achieve this.

The positions of the sensors on the module have to be determined. Internally the structure of the sensors will be well known with an accuracy of about 1-2um. This information is obtained through the production mask drawings of the sensors and accessed through alignment marks on the sensors. The modules will be build on an assembly machine under control of an operator checking the process under a microscope. The expected placing accuracy is 5um. After the modules have been assembled they can be surveyed with an optical survey machine at MIT. The accuracy of this machine is about 10um in-plane. An out-of-plane contrast measurement leads to an accuracy of 50 to 100um.

The same methods as for the module while be used for the ladders. Three modules will be glued to one ladder with an accuracy of about 5um. Then the ladder will optically survey with an in-plane accuracy of 10um and an out-of-plane accuracy of 50 to 100um. After the ladder gets approved it will be shipped to BNL where additional survey can take place. There is a possibility to do this on a coordinate measuring machine and/or by the BNL surveying group using state-of-the-art optical survey equipment.

At BNL the ladders will probably be put together in 2 clamshell cylinders which can be measured on a coordinate measuring machine or by the BNL survey group. After the clamshells have been put together on the ISC to form the IST barrel another survey needs to take place. Up to this point it should be possible to survey the silicon sensors themselves. The sensors have the highest internal accuracy (1-2um) and in the end it is their position which should be known with the best accuracy. However, after the clamshell has been closed visual access to the sensors will become impossible, especially after the ISC gets integrated with the rest of the inner tracking system. It is important to have survey points on the ladders, the clamshell structure and the ISC which are visible to the BNL survey group. These survey points then 'anchor' the IST inside the inner tracking system and finally to the whole STAR detector. It is extremely important that the BNL survey group is involved from the beginning in planning the whole survey process.

Finally the inner tracking system (PIXEL, IST and SSD) get mounted inside of the STAR TPC. Its location will be determined by the BNL surveyors through optical survey.

All the information which has been gathered in the previous steps will be used to do a least squares fit for the positions of the IST silicon sensors. Since there are only 144 sensors it will be possible to do some hand checking and possible correction of the results. These positions will then go into the STAR tracking geometry and acts as a

starting point for software alignment with tracks. This final process can easily take a couple of person months to achieve the desired level of confidence. Therefor every effort should be made to have a sufficiently rigid construction. Removal of the detector will set a physics analysis back by months and should not be undertaken lightly.

0.6 Prototypes, System Tests and Milestones

0.9.1 FY08 R&D

0.9.1.1 Detector module prototype

0.9.1.2 Ladder prototype

0.9.2 FY09 R&D

0.9.2.1 Silicon sensor prototypes

0.9.2.2 Production module prototypes

0.9.2.3 Production ladder prototype

0.9.2.4 Readout system prototype

0.9.3 System tests

0.9.3.1 Module tests

0.9.3.2 Ladder tests

0.9.3.3 Barrel tests

0.9.3.4 System integration tests

0.9.4 Milestones